WET CHEMICAL METALLIZATION OF SILICON SOLAR CELLS: STATUS AND PERSPECTIVE OF INDUSTRIAL APPLICATION

A. Letize, B. Lee, D. Cullen,
MacDermid Enthone Electronics Solutions, Inc. 245 Freight St., Waterbury, Connecticut 06702, USA

ABSTRACT: Formation of electrical conductors by wet chemical metallization is well-known in the electronics industry, with decades of implementation in the fabrication of printed circuit boards and microelectronics. However, its usage in the photovoltaic industry is still in its early stages. As the solar cell fabrication process matures, wet chemical copper metallization will move from acceptable, to preferred, to required. Relative to screen printed silver paste, copper allows higher aspect ratio, self-aligned conductors, and compatibility with increasingly complex materials and processes. Many of the highest efficiency cell architectures already require, or benefit from, wet chemical metallization. Future commodity cells are predicted to require copper conductors, due to the need to continually improve efficiency while simultaneously driving costs lower. This paper is a review of the current status of wet chemical metallization in the photovoltaic space, and a prospectus for where the technology trends are leading. Also included is a brief history of plating in PV, as well as its advantages, challenges, application to specific cell types, and path to mass adoption.
Keywords: copper, wet chemical metallization, electrodeposition, cost reduction

1 INTRODUCTION

Wet chemical metallization via deposition of metals from electrolytes was initially developed in the early 1800s, and continuously refined over the past two hundred years. The technology grew further with the birth of the computer, and today enjoys mass utilization across a wide swath of electronics fabrication processes, including printed circuit boards, semiconductors, and microelectronics. The printed circuit board industry, which relies greatly on plating processes, is over $62 billion dollars today. Despite this, plating has yet to see wide-spread adoption in the photovoltaics industry, although several advantages exist. Still, PV roadmaps expect a growing percentage of cell manufacturing processes to use wet chemical metallization processes in the coming years, based on numerous factors such as efficiency advantages and cost reduction [1].

Solar cell contact formation by screen printing and firing of silver paste is by far the most common method of metallization today. Screen printing has dominated for decades because of process simplicity, high throughput and scalability of the technique. However, silver paste printing has several notable drawbacks. The efficiency of screen printed cells are limited by the capability to print narrow fingers, which is dictated by screen materials and paste rheology. Additionally, the paste firing process is limited in its ability to make low resistance contact to silicon, especially in advanced emitter concepts. Finally, silver paste is significantly more expensive than copper, the primary metal used in solar cell plating processes. Coupled with the inherent volatility in the price of silver, a precious metal, copper plated cells offer an attractive economic proposition. This paper will show how wet chemical metallization offers unique advantages over the incumbent process in each of the aforementioned aspects.

1.1 Metals and deposition methods

Historically, a wide variety of metals and alloys of metals have been utilized in the metal finishing and electronics industries. Most often the metal/alloy is chosen based on the application. Factors such as physical properties (hardness, corrosion resistance, conductivity) as well as cost considerations and compatibility with substrates/superstrates will determine the selection of metal for a particular use. The most frequently used metals in industrial applications include inexpensive transition metals such as nickel, cobalt, copper, tin and zinc, as well as more noble (and expensive) examples such as silver, gold, palladium, and platinum.

Nickel is the most common choice for metal in applications requiring direct contact to silicon, for a few reasons. First, nickel forms a low resistance contact to doped silicon [2]. The contact resistance can be further reduced by thermal annealing at low temperature, which can aid in the formation of nickel silicide intermediates [3]. This step can also aid in adhesive force, discussed later in this work. Finally, nickel is an excellent barrier to diffusion of subsequently plated layers, even at very low thickness [4]. This is especially important, since the most common primary conductor in this application is copper, which can diffuse into the space charge region of doped silicon and increase recombination, lowering the efficiency of the device.

As mentioned, copper is the preferred metal for use as the main conductor in solar cells fabricated with wet chemical metallization. Copper is only slightly more resistive than silver (1.68 μΩ*cm vs. 1.59 μΩ*cm). Combined with the fact that copper is orders of magnitude cheaper than silver, the difference in required metal thickness for equivalent conductance is negligible. In addition to its economic benefit, copper electrodeposition is simple and well understood. Copper is the primary metal conductor deposited in the manufacture of printed circuit boards, as well as a significant portion of semiconductor metallization.

Because copper is susceptible to oxidation, it is normally capped with a 'final finish,' which is typically tin, silver, or an organic solderability preservative (OSP). The final finish layer serves to prevent oxidation of the underlying layer (normally copper) and maintain an oxygen-free surface suitable for bonding in the following soldering/interconnection step of module formation. The layer is normally very thin (as low as 100 nm case of silver), and doesn't add appreciably to the cell performance or cost.

The preceding metals can be applied to a solar cell in a number of different methods, depending on the specifics of the cell design and other manufacturing requirements. Traditionally, plating takes place by either

electroless or electrolytic deposition. Electroless deposition is driven by differences in the galvanic potentials between two (or more) metals in the reaction. This reaction can take place directly by immersion displacement of the base metal by a more noble metal in solution, or through an intermediate reaction step whereby a catalyst drives the reduction of a metal from solution onto the substrate surface. Electrolytic deposition is effected by connecting the surface to be plated to a power source and supplying a source of electrons to the surface, which catalyzes reduction of the metal from solution onto that surface (cathode). An equal and opposite oxidation reaction occurs at the anode surface, which is normally a basket containing the same metal being deposited. By this method, the metal being plated out of solution at the cathode is replenished by dissolution from the anode Another novel method of wet chemical metallization on solar cells, described in detail by Bartsch [5], is light induced plating (LIP). The general principle of LIP is that the cell is illuminated during the deposition process and simultaneously contacted with a power source at the rear (non-plating region) of the cell. In this way, the incident light intensity on the cell surface drives the rate of metal deposition, and a uniform layer of metal is deposited on the cell in the predefined pattern. Using the proper combination of chemistry, equipment and process control, high throughput and excellent efficiency results are achievable on plated solar cells [6].

1.2 Pattern formation and plating equipment

Before wet chemical metallization can be applied to solar cells, the pattern to be plated must first be defined. In some metallization processes, the first metal contact layer is applied by a physical vapor deposition (PVD) technique such as evaporation or sputtering. After a thin, conductive layer is applied to the wafers surface, its pattern is defined by one of several lithographic techniques, such as print and etch of a screened resist, or photoresist application followed by expose/develop/etch/strip. The end result is that the metal seed layer remains only in the pattern defined for further metallization (ie. H-grid with 50 micron fingers). This patterning technique is most common for silicon heterojunction (SHJ) and interdigitated back contact (IBC) cell concepts.

For direct metallization of silicon without use of a PVD seed layer, laser patterning is the method of choice. During laser-defined patterning, the primary objective is to remove the passivation layer(s) on the surface of the cell, which may include silicon nitride antireflective coatings as well as silicon oxide dielectric layers. Once the dielectric is removed by laser ablation, the underlying silicon can be plated by the methods mentioned above. Laser patterning technology has progressed significantly over the years, from buried groove contacts [7] to laser doped selective emitters (LDSE) [8], laser chemical processing (LCP) [9], nanosecond laser ablation, and finally picosecond laser ablation, which can optionally include doping for lightly doped and/or boron emitters. The advantages and challenges of the different laser patterning techniques will be discussed below.

In order to achieve the desired results as it relates to wet chemical metallization of solar cells, it is critical to have a proven combination of chemistry and equipment. Although plating can be applied by numerous techniques, industrial production demands a simple, reliable and high throughput set of equipment. For this reason, the most common tools employed in production are conveyorized, high volume manufacturing units. Equipment manufacturer RENA offers a horizontal conveyorized unit capable of single-sided wetting and throughput in excess of 3000 wafers per hour (figure 1). Besi (Meco) offers a vertical unit for simultaneous plating of front and back of wafers, especially useful for n-type bifacial or heterojunction wafers. Innolas supplies HVM laser solutions for patterning prior to plating.

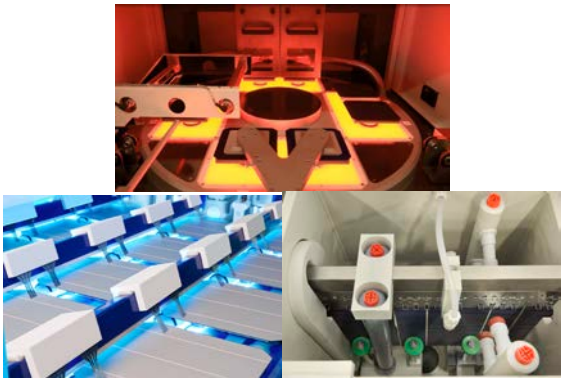

Figure 1: (Above) high speed picosecond laser processing tool from Innolas; Inline, conveyorized high volume plating tools are available from RENA (left) and Meco (right)

2 ADVANTAGES OF PLATING

As manufacturers strive to achieve ever higher efficiency results at a competitive cost, implementing plating for both efficiency benefits and cost reductions will become the obvious choice.

2.1 Increased Jsc / reduced shading

Screen printed silver paste has a number of well known drawbacks. It is difficult to achieve finger widths below 50 microns with sufficient conductivity due to the constraints of screen printing technology. Additionally, printing such narrow contacts runs the risk of insufficient laydown, line breaks and other reliability issues. Alternative printing methods, such as double printing and use of stencils, can improve these issues, but do so at a cost of additional printing/drying steps and consumables. On the other hand, laser defined patterns can produce fully-plated contacts with finger widths of less than 30 microns (figure 2), which can significantly reduce shading and thus increase the J_{sc}. It has been shown that J_{sc} values in excess of 40 mA/cm^2 can be achieved using laser-defined and plated patterns [10]. Also, the effective optical width of plated conductors is less than paste, due to the internal reflectance of rounded copper traces [11].

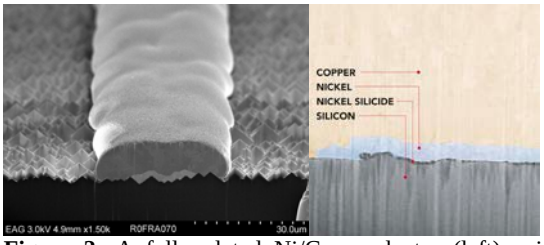

Figure 2: A fully plated Ni/Cu conductor (left), with finger width of less than 30 µm; 100% contact of plated nickel to silicon (right), leading to low R_{ser}.

2.2 Improved electrical contact

Direct plating of nickel to silicon also carries the advantage of improved contact resistance when compared to screen printed silver paste. Printed and fired paste relies on the formation of spot-contacts consisting of silver-glass crystallites, which are inherently not very conductive, and require high surface concentration of phosphorus to make acceptable contact [12]. In contrast, plated nickel forms a continuous contact to the silicon surface. Annealing of the plated deposit can result in nickel silicide formation, which further reduces contact and series resistance. It has been shown that plated nickel forms a lower contact resistance to doped silicon (figure 3) [13], and is especially advantageous in combination with lower phosphorous doping. The quality of the contact results in higher fill factors than paste, consistently higher than 80%, and a very narrow distribution of cell efficiencies within a group of plated cells, which results in less cell groups during binning [14]. There is also difficulty in contacting boron-doped emitters with silver paste, something which may be overcome by forming nickel contacts to the emitter.

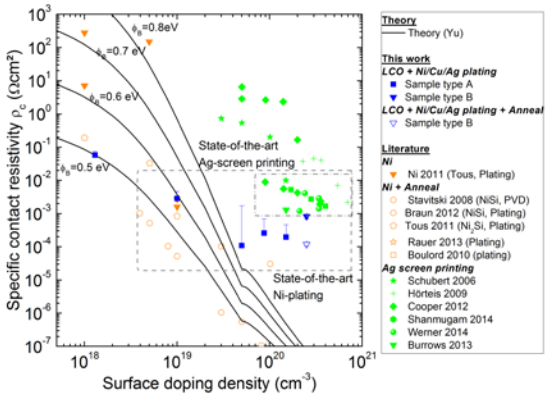

Figure 3: Comparison of contact resistivity for plated nickel and silver paste on phosphorus doped emitters, demonstrating the superior contact resistivity of nickel [13].

2.3 Reduced cost and price volatility

Finally, a major advantage of plating that can't be overstated is the cost savings when compared to paste. Spot price comparisons show that silver has averaged approximately 100X the cost of copper historically. As a result, silver paste is a significant portion (>10%) of the cell's bill of materials. Additionally, it is proposed that the cost of Ag will be materially impacted by expansion in the PV industry, even taking into account the expected reduction in usage per cell [15]. Finally, fluctuations in the price of silver, a precious metal, have a disrupting effect on manufacturers' costs, inventory, and supply contracts. All of these issues can be solved by switching to copper, a cheap, commodity metal (figure 4).

3 CELL TYPES

3.1 p-type BSF / PERC

P-type, Aluminum back surface field (BSF) crystalline silicon cells represent the current standard for industrial commodity cells, and account for nearly 90% of production as of 2015 [1]. As such, the application of plating to BSF cells has been a focus of research for years. BP Solar introduced the "Saturn" cell, featuring buried groove plated contacts, and manufactured this cell type in mass production for a decade [16]. Later, Suntech adopted a similar technology and created the "Pluto" cell, featuring LDSE patterning and plating in combination with a passivated rear [17]. At the same time, much research was going on at major institutes, manufacturers and industry suppliers to understand and progress the use of plating in solar cell manufacturing. Initially, light induced plating was used in combination with a silver paste seed layer, in order to gain some benefits of plating while still maintaining sufficient adhesion to the wafer [18]. After equipment and process improvements made it possible to plate directly to silicon after a simple laser ablation pattern step, many new wafers with high efficiency and good adhesion/reliability were created by a number of institutes and companies, detailed later in this work. Using this technology, a turnkey solution was created for patterning, plating and annealing of standard BSF or PERC cells with a simple, inline process with efficiencies above 19.5% in production on Cz silicon [19].

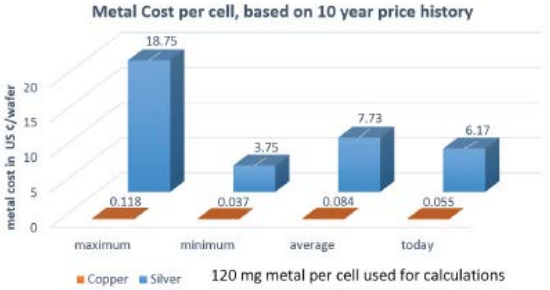

Figure 4: Metal cost per cell based on spot price of the conductor metal (Cu vs Ag) over the past 10 years, demonstrating the volatility in silver usage costs.

In recent years, standard cell production has begun shifting to the use of a rear passivation scheme to create PERC (passivated emitter and rear cell) designs. The PERC process is a relatively simple upgrade from BSF, requiring application and patterning of a rear side passivation layer, followed by standard front side metallization. Therefore, plating can be just as easily applied to the PERC cell concept. In fact, the vast reduction of rear side recombination by passivation once again directs the attention to the front side, where narrow plated conductors have the potential to realize even further gains in efficiency [20]. Plating was successfully applied in the Pluto cell mentioned above, as well as the 'i-PERC' cell concept by Russell, et al. [21], and further improved upon in subsequent testing, demonstrating efficiencies up to 20.7% [22]. Cornagliotti et. al demonstrated a 0.5% absolute efficiency improvement over screen printed paste for a plated PERC cell [23]. Additionally, the use of laser doping (selective emitter) during the front side patterning step can push the efficiency above 21% [24].

3.2 n-type PERT / bifacial

Historically, the highest efficiency cells have been fabricated using n-type silicon base material with boron-doped emitters. This is because n-type Si is not susceptible to potential induced degradation (PID) and light induced degradation (LID), which has negatively impacted p-type Si cells, although the recent practice of regeneration has resulted in efficiency recovery in these

cells. N-type silicon fabrication processes can be combined with plating much like p-type cells mentioned above, with a couple key differences. First, n-type cells feature a boron emitter, as mentioned, which is more difficult to make a low-resistance contact to, especially with standard silver paste. This difficulty can be overcome by forming a selective emitter prior to patterning and plating the cell. Also, n-type cells often feature a patterned grid on both sides (bifacial design), so it is important to have a double-sided contact and plating method. It has been shown that the application of plating to an n-PERT cell (passivated emitter, rear totally-diffused) can improve efficiency by 0.4% absolute over printed paste [10]. When combined with a front side selective emitter, achieved by laser doping, the efficiency of this cell design is improved even further. Uruena et. al reported an efficiency improvement from 20.8% to 22.0% by use of laser doping, and a champion cell of 22.5% [25]. Mondon reported similar efficiencies when combined with the PassDop rear passivation process [26]. First Solar (TetraSun) has recently reported average high volume production cell efficiency in the 22% range using a unique n-type bifacial cell architecture with nickel and copper plating [27].

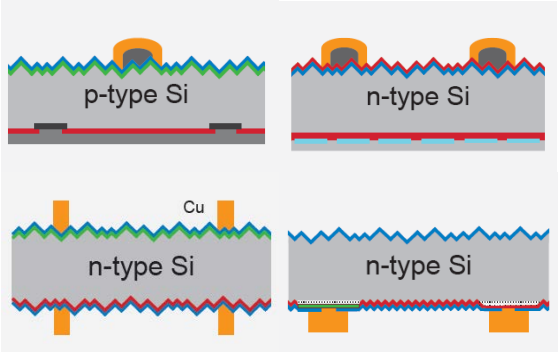

Figure 5: Schematics of p-PERC (top left), n-PERT (top right, SHJ (lower left), and IBC (lower right), featuring copper as the primary conductor.

3.3 Silicon heterojunction

Another area of intense research in recent years is the silicon heterojunction (SHJ) cell type, sometimes called heterojunction with intrinsic thin-layer (HIT). SHJ cells differ from other n-type designs in that they feature layers of amorphous silicon that serve as passivating films with a wider bandgap. These semiconducting films greatly reduce recombination at the junction interface, which leads to extremely high Voc levels for these cells [28]. The unique opportunities of heterojunction cells also come with unique drawbacks. Due to the presence of these thin amorphous silicon layers, the cell efficiency is severely damaged by high temperature (>200 ºC) thermal processes. As a result, the use of silver paste as the primary conductor is not ideal; since the paste can't be fired as in a standard process, SHJ cells require much higher quantities of a thick film-like paste that is annealed at lower temperature. Cells require more than 200 mg of silver paste for monofacial designs and over 350 mg for bifacial designs in order to achieve acceptable conductivity [29]. Also, the higher quantity of paste leads to higher shading than desired. The special challenges of the heterojunction cell, therefore, make the application of wet chemical metallization especially attractive. Plating is achieved at low temperatures (typically onto a PVD seed layer), and through a resist mask, thus creating a conductor grid with high aspect ratio and excellent conductivity. Companies such as Kaneka and Panasonic have reported lab efficiencies of 25.1%, and 25.6%, respectively, by combining a heterojunction design with copper plating in a back contact configuration [30, 31]. Solar City (Silevo) has achieved efficiencies over 23% on a bifacial SHJ concept, and is currently scaling this process for mass production [32].

3.4 Interdigitated back contact

The final cell type that can benefit from wet chemical deposition is interdigitated back contact (IBC) cells. In fact, the only mass produced IBC cells have featured plating, and it can be argued that the cell design *requires* plated conductors for performance. Due to the presence of both p- and n-doped regions on the same side of the wafer, IBC cell manufacturing comprises a complex process. This process includes two separate diffusion steps, multiple lithography sequences, and copper and tin plating to form the conductors. The primary reason that wet chemical metallization is employed on IBC cells is that the conductors must be very thick (35-50 microns thick) because the effective 'finger length' spans the total length of the wafer in this cell design. Also, warpage is critical since the metallization is only on one side. IBC cells have been mass produced solely by SunPower over the past 20 years, and have consistently been the highest performing modules in the field over this time. Davis et. al have demonstrated a 25.0% efficient 4" wafer, while Trina has produced a 6" R&D cell with efficiency of 23.5% [33, 34].

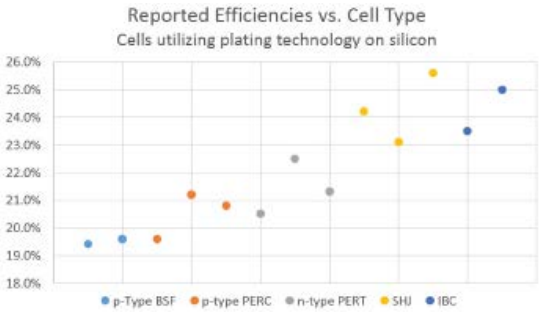

Figure 6: Recent results for cell efficiencies obtained with wet chemical metallizaiton on full-area cells, using easily scalable manufacturing processes [10, 12, 24-26, 31-37].

4 CHALLENGES

As this work has demonstrated, there are a number of advantages to adopting wet chemical metallization for the production of solar cells across various cell types. However, there are also some challenges associated with this transition. First, implementation of a new metallization process requires substantial capital expenditure, which makes it more difficult to immediately realize the economic benefit of copper conductors. Also, replacing a well known process with a new set of lesser known metallization steps may be unattractive to a risk-averse industry that prefers the 'fast-follower' approach. The slow adoption of plating in PV manufacturing can be attributed to these obstacles, as well as some of the technical challenges detailed below.

4.1 Adhesion

Ever since research has focused on replacing paste with plated contacts for solar cells, the adhesion of the plated stack to the silicon substrate has been a primary obstacle to success. For obvious reasons, adhesion failure between the seed plated layer and silicon would lead to performance and reliability failures in the field. As mentioned earlier in this paper, techniques such as laser groove buried contacts overcame this issue mechanically by metallizing a trench [7]. Also, the formation of a nickel silicide layer by thermal annealing after plating was examined for its adhesive properties [38]. The improvement of laser ablation patterning process, especially the introduction of picosecond pulse lengths, has also led to an improvement in adhesion (figure 7). This is presumably due to a rougher Si surface that serves as an anchor point [19, 26]. Some techniques actually involve intentional lasering of "anchor points" to serve as adhesion promoters [36]. The sum total of this work is that very impressive adhesion results have been presented by numerous sources detailed here, with 90' peel strengths greater than 1.5 N/mm becoming the norm. It is the author's opinion that plated adhesion will no longer be a significant obstacle for the industry going forward.

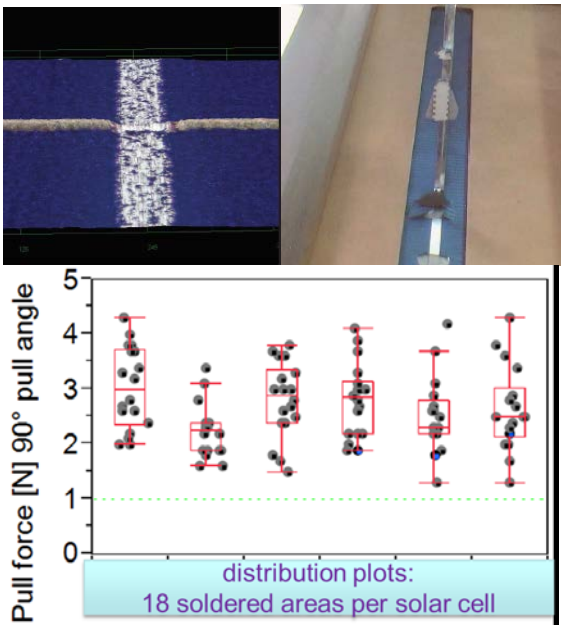

Figure 7: Demonstration of plated finger adhesion during shear testing (left); High soldered busbar adhesion leading to silicon fracture during 90º peel test (right). Box plots of peel testing also show excellent adhesion results [35].

4.2 Background plating

Another challenge to the mass adoption of wet chemical metallization has been the issue of background plating. A number of studies have focused on the causes and methods of prevention for background plating [39, 40, 41]. Background plating generally occurs when an interruption in the passivation layer covering the surface to be plated allows the silicon to plate up in undesired locations. Background plating leads to increased shading and lower J_{sc}, but generally does not cause shunting, since the barrier metal will plate in the unwanted areas as well, preventing diffusion of copper into the SCR. The primary causes of background plating occur during the wafer texturing, cleaning, and passivation steps. Impurities or other fragments are not properly cleaned from the silicon surface, and thus introduce defects in the passivated surface, which is able to plate in subsequent metallization steps. Also, micro-cracks caused by stress sometimes leave voids at the base of pyramids, which can then plate. Finally, scratching of the silicon nitride passivation layer (by excessive handling or equipment) can remove the passivation layer in regions of the cell, which will also cause background plating. The problem of background plating is an ongoing issue, but can be greatly reduced by controlling the wafer cleaning and passivation processes. In the case of direct plating on silicon, the choice of silicon activation chemistry and proper control of the pretreatment process is also critical to the incidence of background plating.

4.3 Long-term reliability

One of the greatest impediments to implementing wet chemical metallization is concerns over long-term reliability of plated cells and modules. This stems from two sources: the fear of copper penetrating into the emitter region and degrading efficiency, and the fear that, over the long term, plated conductors may delaminate and/or corrode, leading to a similar module failure. To address the first concern, numerous works have been published which demonstrate that nickel is an excellent barrier to copper diffusion. The barrier properties of nickel are also well known from the semiconductor industry. Bartsch's method of accelerated aging uses Arrhenius plots to extrapolate the time-to-failure (5% power loss) for a given metallization stack at a particular temperature [42]. Using this method, even a very thin nickel deposit should be a suitable barrier to copper diffusion for over 100 years on a rooftop [43]. In addition to this method, there are a suite of accelerated aging tests for modules specified by IEC method 61215. These include thermal cycling, damp-heat exposure, humidity freeze, and mechanical load testing. The majority of the plated cells mentioned in this paper were put through IEC testing and easily passed, some even running far beyond the required limit of cycles or time [12, 21, 32, 35]. However, perhaps the greatest proof, so far, of long-term reliability on plated modules is the ongoing study of BP Saturn modules in the field [44]. Power data gathered from Saturn modules shows remarkably high power output after 20 years of operation, demonstrating that plated modules may be just as reliable as silver paste long-term.

5 SUMMARY

There are a number of potential advantages that can be gained by switching to plated contacts. The advantages, which include lower shading, lower contact resistance, and lower cost, have been laid out in this review, and supported by the numerous works cited here. Efficiencies in excess of 20% have been achieved using applications of wet chemical metallization on various cells types. Additionally, equipment and process improvements have led to excellent adhesion, elimination of background plating, and long-term reliability in modules featuring wet chemical metallization. Plating now offers a simple and reliable solution for simultaneous efficiency improvement and cost reduction.

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