CONTROLLING COPPER ROUGHNESS TO ENHANCE SURFACE FINISH PERFORMANCE

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ABSTRACT
Printed circuit board design and expected performance is driven today by three main markets; high functioning portable devices, infrastructure to support these portables and the ever increasing demand from the automotive industry for increased electronic content in automobiles. These technology areas both require ultra-high density design, high signal speed capabilities and tolerance to high thermal exposure both during assembly and in ultimate end use. The design and performance requirements present significant challenges for the Printed Wiring Board (PWB) manufacturer.

Soldermask adhesion to copper is a key factor to be considered. PWB's for the types of applications detailed above are frequently subjected to aggressive surface finish chemistry plus multiple lead free reflow excursions and yet still must demonstrate reliable performance in unpredictable and hostile end use environments. The use of older traditional treatments prior to soldermask application resulted in inconsistent adhesion, which ultimately resulted in compromised product reliability. In general, and almost universally, board manufacturers today use proprietary adhesion promoting products that impart a significant degree of surface roughness to the substrate prior to soldermask application for some portion of their production. These proprietary process cycles result in enhanced and more uniform soldermask adhesion. This improved adhesion results in many obvious performance and design benefits satisfying Original Equipment Manufacturers (OEM's) ultimate goal of producing consistent, reliable and robust products.

Soldermask adhesion promoting products, as mentioned, typically involve the use of a chemical process that modifies the copper substrate topography to a considerable degree, thereby creating an overall high degree of surface roughness [1]. This naturally results in a significantly increased real surface area to which the soldermask can then anchor more firmly and consistently, resulting in enhanced adhesion. The downside to having a substrate with high surface roughness is that this can result in challenges when applying the subsequent final surface finish. These challenges frequently manifest themselves in terms of difficulties in achieving good surface cleanliness prior to surface finish application and also degraded solderability of that surface finish. This is particularly the case for thin surface finishes, such as, immersion silver processes.

This paper expands on work previously reported which proposed a roughness reducing step prior to thin surface finish application for improved product performance and superior reliability [2]. The work discussed here expands upon the benefits associated with soldermask adhesion promotion and also focuses further on how the use of a substrate roughness reducing process step after soldermask application can mitigate the negatives associated with high surface roughness and successful final surface finish application.

INTRODUCTION
Classically, there are a few ways to prepare a copper surface prior to soldermask application. Each method commonly employed today, both chemical and/or mechanical, result in a significantly roughened surface [1];

- Jet pumice which imparts a slurry of pumice in water either brushed or sprayed onto the copper surface.
- Silica or alumina oxide treatment
- Mechanical brush scrubbing
- Simple chemical cleaning in the form of a microetch designed to deliver a tooth-like structure to the copper surface.

There are both positive and negative process and performance characteristics associated with each of the techniques listed above. Facility audits of fabrication houses frequently show that more than one of the roughening processes outlined are commonly utilized concurrently in everyday production at individual manufacturing sites. Why this is the case and why one process is chosen over another for any specific job type being processed is not obvious. What is regularly noted however is that end users, board fabricators and chemical suppliers have seen the need for more consistent, homogeneous, robust surface roughening techniques to be developed beyond those listed above. The basic reasons for this lie in the short comings of the existing processes, for example; pumice and silica can create a non-uniform roughness potentially embedding particles into the copper surface if not properly maintained. Brush scrubbing also suffers inconsistencies when the brushes are not properly maintained. Chemical etching becomes more aggressive as copper ion concentration builds in the bath. All of these changes which occur over time and use can be mitigated by employing correct maintenance procedures, however there is still significant potential that any resultant surface may

not provide the necessary uniformity and the specific degree of copper roughness for optimal soldermask adhesion to withstand localized and/or high thermal exposures.

In an attempt to mitigate these issues even further fabricators regularly employ proprietary chemical soldermask adhesion promotion processes (SMAP). These provide a combination of both high surface roughness and a degree of chemical bonding which results in superior mask adhesion [1, 3].

Though there are a number of chemical suppliers providing such technology, it was decided for this body of work to focus on one market leading product and test the effect of varying line processing speeds which necessarily translates to different substrate etch depths. The etch depth is clearly the main control parameter for such process chemistries. For the specific chemical process and equipment set chosen for this work, the chemical supplier typically recommends as optimum a 3.2m/min conveyor speed.

As mentioned in the previous paper, even the same proprietary chemical formulation used with different processing parameters, such as time and etch depth, will create very different surface topography. Figures 1(a-c), illustrate the topography created by the chosen chemical soldermask adhesion process, when employed at three different conveyor speeds; 2.0, 3.2 and 4.0m/min.

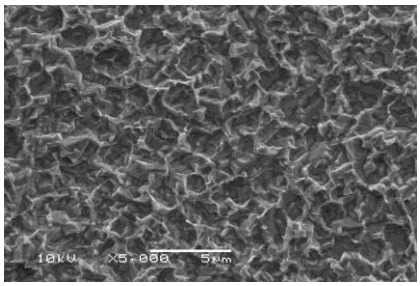


Figure 1a: SEM of copper surface after soldermask pretreatment at 2.0m/min conveyor speed

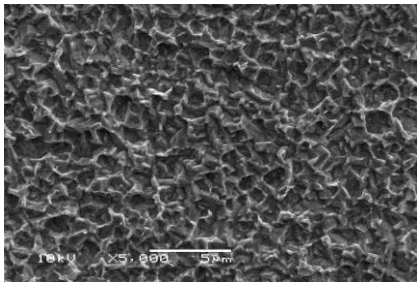


Figure 1b: SEM of copper surface after soldermask pretreatment at 3.2m/min conveyor speed

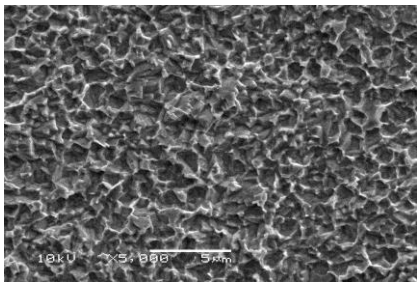


Figure 1c: SEM of copper surface after soldermask pretreatment at 4.0m/min conveyor speed

For comparison, Figure 2 shows the roughness created by a conventional process which in this case was a mechanical brush followed by 20 micro inch copper removal in a hydrogen peroxide/sulfuric acid microetch soldermask adhesion pretreatment. It is evident just from visual observation that the resulting roughness is dramatically less. The advantages of creating a strong bond between the copper substrate and soldermask by significantly roughing the surface are clear, however, what needs to be explored more is the challenges that arise as a result of this roughening step.

When SMAP type processes were initially introduced they were typically used in conjunction with electroless nickel/immersion gold (ENIG) solderable surface finish. The high nickel thickness mitigated the negative effects of very high copper roughness, so the negatives associated with these processes were not immediately obvious to the industry.

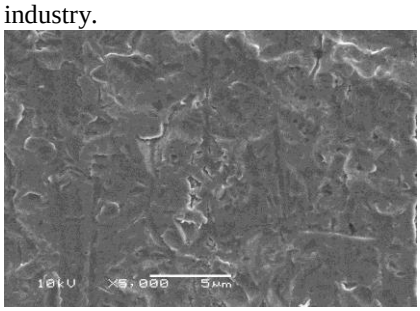


Figure 2: SEM of copper surface after pumice soldermask pretreatment

This paper compares the performance characteristics of thin, metallic solderable surface finishes, with and without the use of a roughness reducing step(s) which is used to reduce the very high degree of surface topography prior to their application.

Soldermask and Adhesion Promotion

The drivers for the requiring the use of a chemical proprietary SMAP include the ever finer lines and spaces that are frequently now employed; reducing the copper trace width reduces the available area to anchor the soldermask.

Immersion tin has been heavily adopted by the automotive industry, as the electronics content in the automobile grows [4]. One challenge end users see with immersion tin is the required deposit thickness to withstand multiple assembly

cycles. OEMs are currently demanding 1.2 microns of pure tin, as plated. This requires extended board contact time in a hot and chemically aggressive plating bath. Although this thickness requirement is only 20% greater than the usual industry standard of 1.0 micron tin thickness, this results in the fact that increased exposure time to the chemical bath can be at least a further 40%. This increased exposure to the aggressive plating bath is one reason why the use of advanced soldermask adhesion promotion processes is being instituted regularly.

In addition to the above, some board designs require localized solder fountains during fabrication which can embrittle or lift the soldermask.

Also, end use applications of PCB's within an automobile, especially engine control, can result in the board being subjected to very high thermal exposure on a frequent basis. When plating relatively thin immersion metal layers such as silver or tin, the metal is conformal to the existing topography of the underlying copper substrate. If the plating metal cannot properly cover the copper due to excessive roughness performance issues such as discoloration, premature tarnish, degraded solderability and sometimes microvoiding may occur.

Surface Roughness Analysis

As detailed above, SEM investigations will give some qualitative information on surface roughness, however it can be quantitatively analyzed using 3D Optical Surface Profilers. A noncontact method [5] using white light interferometry to measure surface roughness was utilized for this experimentation. This instrument was again used as an investigative tool to understand the roughness created by the SMAP and how this was subsequently altered after the roughness reducing steps was applied. Specific details of the technology and measuring techniques can be found in the previous paper [2].

Surface characterization methods in engineering have used Ra most commonly. This is defined as the average surface roughness or average deviation, of all points from a plane fit to the test part [5].

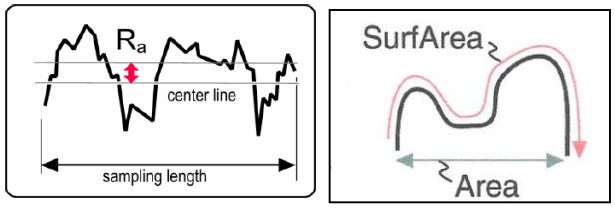


Figure 3: Schematics of roughness terms: Ra and RSAR

It is clear however that a simple Ra measurement misses a significant amount of important information for understanding surface roughness especially in the case of printed circuit boards. The analysis measurement of choice is Surface Area Ratio or RSAR. Figure 4, below, explains how an RSAR number is determined. This is, importantly, a measurement of the degree of micro roughness found within the overall macro roughness of the test substrate. It can educate the analyst on micro topography which occurs along the larger peaks and valleys within the general topography of the sample under investigation [5].

$$RSAR = \frac{Measured\ surface\ area}{Area\ of\ a\ flat\ plane\ of\ same\ xy\ dimension} - 1$$

Figure 4: RSAR calculation

For example, the measurements taken for this project were over a square area of 177x134 microns (figure 5). This is a geometric area of 23,718 square microns. The measured RSAR number is a quantitative measurement of the additional (real) surface area, rather than simply the basic geometric area of a test sample.

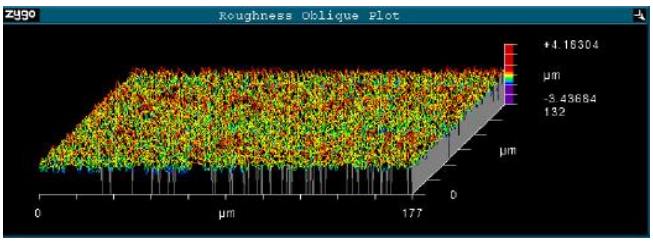


Figure 5: Example of zgyo graph

Surface Finish Thickness Measurements

It has been well documented through IPC, end users and chemical suppliers that the plated surface finish thickness is extremely important to achieving desired shelf life and functional performance. Thickness recommendations for various surface finishes can be found in IPC standards, OEMs design/build specifications and your process chemistries' Operating Guides. Ultimately, end users understand their desired performance in specific environments so it is up to the OEM to relay their expected surface finish thickness targets. It is the responsibility of the board fabricator to ensure that they have the latest technology in thickness measurement techniques. This does not mean a constant need to purchase new equipment but it does require annual calibrations and daily checks of the metal thickness standards.

X-ray Fluorescence (XRF)

Today's most predominant measurement method for metal deposit thickness is X-ray Fluorescence. The plated metal surface is bombarded with high energy x-rays, the excitation of these rays emit back to a detector identifying the quantity of metal ions on the surface of the deposit. The underlying copper metal is calibrated into the program to ensure only surface metal is being analyzed. Difficulty may arise when plated metal deposits are very thin or more importantly where multiple layers of different metals are present. Calibrated thickness standards within the range of your specified deposit thickness target will result in the most accurate thickness readings. One must use standards that fall on the high and low end of your specification to create a linear regression for the equipment. It is also important to

utilize the correct collimator size for your measurement pad. These guidelines can be found in the instrument operating manuals and there is also some guidance offered in IPC specifications. Collimators that are too large for the measurement pad will result in inaccurate readings due to background scatter from the soldermask, laminate and adjacent metal pads. A good rule of thumb is the pad should be at least three times the size of the collimator. XRF equipment guidelines should be followed.

For immersion tin deposits, hold times or heat treatments will affect the measured pure tin thickness when studied by XRF. During heat exposure copper-tin intermetallic layer growth is accelerated and there is a significant loss of pure tin to the underlying copper in the form of intermetallic compounds (IMC). Combinations include Cu_6Sn_5 and Cu_3Sn, as shown in figure 6, which details the typical copper and tin interactions when these metals are in direct contact [6]. XRF programs do not normally exclude the tin in the IMC layer. Readings capture "total" tin, i.e., that present as pure tin and that contained within the IMC layer. This data is not valuable, as the pure tin left on the PCB surface is of greatest importance for solderability performance. To fully understand the pure tin thickness produced in this test Sequential Electrochemical Reduction Analysis was employed.

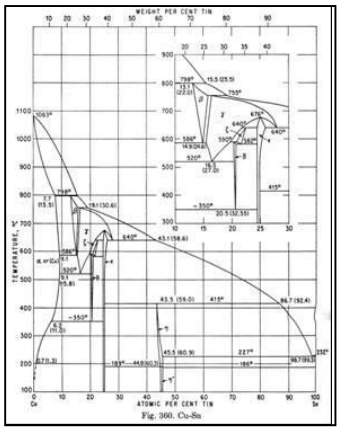


Figure 6: Phase diagram of tin and copper

Sequential Electrochemical Reduction Analysis (SERA)

This more accurate method of measuring pure tin metal thickness, though destructive, uses coulometric reduction. Through the implementation of Faraday's Law and an applied current, the instrument solubilizes the surface metals and distinguishes each layer as the potential of the dissolved material changes. It is then calculated into thickness using textbook densities. For this research, ECI Technology's Sequential Electrochemical Reduction Analysis (SERA) unit was used [7]. This equipment separates pure tin and the two IMC layers associated to immersion tin plating. This instrumentation produces a well defined understanding of the constituents of the plated deposit and details clearly any change or loss of pure tin deposit after heat treatments and/or hold time.

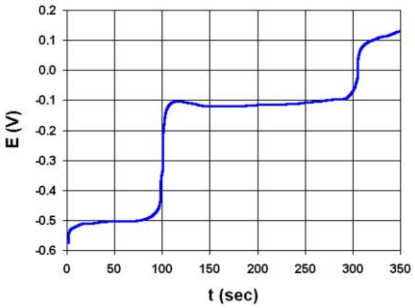


Figure 7: Example of immersion tin SERA graph

A closer look at the resultant SERA graphs in figure 7 reveal, a plateau for the pure tin thickness, this first step in the potential correlates to tin metal. As the instrument detects a potential change, the graph shifts creating the second plateau correlating to the thickness of the Cu_6Sn_5 IMC layer known as the n-phase. A third change in potential correlates to the Cu_3Sn IMC known as the p-phase. The last potential reached is that of copper metal and the measurement test is complete.

PERFORMANCE TESTING

To prove the reliability of their work, PCB fabricators execute a series of tests throughout the manufacture process. For all process cycles, fabricators ensure the chemicals used are in proper specification and that the chemical and mechanical parameters employed follow the chemical suppliers' data sheets and best practice operating guides. In addition physical performance tests based on IPC specification and end user requirements are run to analyze soldermask and surface finish performance. The following tests are examples of those performance investigations especially critical for the understanding of this work.

Adhesion Tape Testing

Though it is seen as a very basic test which is easy to execute, the soldermask adhesion by IPC TM 650 2.4.1 is a reasonable indication of soldermask performance as applied. Issues associated to passing the tape test will be aggravated by subsequent chemical processing or high heat exposure. In this check, a 3M 600 tape 1/2 inch wide is placed over an area on the printed circuit board with both soldermask and defined circuitry. The tape is pressed securely onto the soldermask surface to ensure good tape adhesion. The tape is then removed swiftly on an angle to the panel and observed for any soldermask then adhered to the tape [8]. It can be helpful to place the tape on a white paper background to observe the level of mask removal. No soldermask should be removed from the PCB surface.

Solderability

The main performance criteria of a surface finish is to protect the underlying copper and to ensure successful subsequent assembly of electrical components. Today's market is weighted in surface mount technology executed by printing lead free, normally SAC305 solder paste on the board surface, placing components and reflowing the PCB through a convection reflow oven.

On site solderability tests vary significantly from one customer to the next. The chosen method depends on their volumes, product classification such as Class1, 2, or 3 and end user imposed testing at the fabrication level.

IPC TM-650 provides a host of solderability test methods including but not limited to; edge dip, float, wave solder, solder paste wetting, solderability of metallic surfaces, all of which are tools to demonstrate a level of understanding for a "go/no go" performance of the finished board prior to release for full assembly. As designs become more intricate and the end use performance more critical, physical printing of a production style panel with a stencil which is then processed through a reflow profile can be employed. Close attention should be paid to stencil thickness, aperture size, and applied pressure during pasting and thorough cleaning of the stencil after use. One must be realistic with hand stenciling, the resolution achieved with automated solder paste printing will never be achieved manually and care needs to be made when concluding on solderability performance. For this work, parts were sent for production assembly without components. Also, solder spread testing was used on the immersion tin panels to provide further information. This will be further discussed in the results section of this paper.

PROPOSAL/PAST FINDINGS

In the previous publication, we proposed a chemical step to reduce high copper roughness caused by proprietary soldermask adhesion promoters. It was documented that the SMAP was successful in creating a strong anchor for the soldermask which subsequently prevented chemical attack by both immersion tin and immersion silver processing. It was also shown that high copper roughness without any reducing step degraded the solder spread performance. The present test matrix further explores the effects of high copper roughness on performance characteristics and illustrates the benefits achieved when a roughness reducing step is employed prior to surface finishing.

For this work two specific roughness reducing steps were investigated as well as the surface polishing delivered by the microetch step in the final finish process. For the roughness reducing etch (RRE) explored in the last paper, this bath is designed to reduce the peak to valley roughness and minimize micro topography incorporated within the macro topography, i.e., both Ra and Rsar.

The etch chemistry is single component bath applied horizontally in spray mode at about 25°C for 60 seconds. Based on the performance and findings in the previous work, the RRE was revisited and for each SMAP condition, copper removal in the RRE was kept constant at 40 microinches (1 micron). It was determined that this etch depth regardless of the initial roughness produced by the SMAP process, would produce the optimum surface roughness reduction prior to immersion silver plating.

The second methodology investigated was a jet pumice step incorporated into the front end of a standard immersion silver process. This is also designed to minimize surface roughness. Jet pumice forces by spray pressure, beads of material at the copper surface which when applied properly can result in a smoother, more polished copper surface. For this testing the jet pressure was set to 2.5kg with a 220 grade aluminum oxide solid at 20% in water. The panels were thus exposed for 45 seconds at ambient temperature.

Leading chemical suppliers for immersion silver frequently stress the importance of a smooth copper surface prior to immersion silver finishing [12]. A typical deposit thickness employed is less than 0.5 microns, which is by necessity conformal to the underlying copper, so the resultant surface roughness after silver plating is very similar to that of the initial copper substrate and if this surface roughness is excessive then subsequent solderability, wire bondability and tarnish resistance will be compromised.

For this work two specific types of printed circuit boards were manufactured. One, a MacDermid laboratory test vehicle known as the "Super Coupon". This is a double sided PCB with FR4 laminate at a thickness of 1.6mm. The second design chosen was common to a number of PCB fabricators regular production. Though not a design that specifically requires a special soldermask adhesion promoter, it is a mass production board that is routinely processed through immersion silver surface finishing. This second board design also allowed for production style assembly.

The panels were run through their standard fabrication steps up to the soldermask pretreatment. As a control, brush scrubbing was followed by a 20 micro inch (0.5 micron) etch using a hydrogen peroxide/sulfuric acid solution. The test set was processes through a leading soldermask adhesion promoter process in a production environment. The chemical process supplier recommended 3.2 m/min as the optimum line processing speed, however in this evaluation the test parts were processed at 2.0, 3.2 and 4.0m/min.

Following soldermask application parts were processed through immersion silver and immersion tin plating. To expand on the work from the last paper it was decided to test two immersion tin processes. Figure 8 lists the chemical steps for each surface finish processing cycle. Product names have been removed but the purpose of each chemical bath is described.

Metal Plating Process Cycles

Chemical Process Step	ImmAg	ImmSn A	ImmSn E
Pretreatment	Jet pumice	UV Bump	UV Bump
Cleaner	Alkaline	Acidic	Acidic
	Rinse	Rinse	Rinse
Microetch	Modified persulfate	persulfate	Persulfate
	Rinse	Rinse	Rinse
Copper conditioner	Predip	Conditioner	Predip
			Rinse
Plating Bath	Immersion Ag	Immersion Sn	Immersion Sn
	Rinse	Rinse	Rinse
	Ionic Cleaner	Ioinc cleaner	Ionic Cleaner
	Dry	Rinse	Rinse
	Anti-tarnish	Anti-tarnish	Anti-tarnish
	Rinse	Rinse	Rinse
	Dry	Dry	Dry

Figure 8: Process cycles for immersion silver and tins

EXPERIMENTAL PROCEDURE

The previous publication discussed that there are multiple adhesion promotion formulations available on the market. By altering the process parameters, one chemical set could result in significantly different roughness.

Figure 9, provides an overview of the test matrix for this experimentation. The "standard" surface preparation listed in the top rows utilizes two sets of mechanical brushes at 800 &1000 (one set each) then a brief peroxide/sulfuric microetch of ~20 microinches) prior to soldermask application. This soldermask pretreatment was used as a control for both the immersion silver and immersion tin sets. The next rows show the introduction of the soldermask adhesion promoter. This adhesion promoter is run in production with an optimum conveyor speed of 3.2 m/min. For a broader understanding of roughness effects, as mentioned above parts were also processed above and below this speed at 2.0m/min (high) which would slow the conveyor down remove more surface copper and result in higher surface roughness as well as speeding the line up to 4.0 m/min (low) which would remove less copper and deliver a slightly smother copper surface. Again, it should be noted that fabricators monitor and control their adhesion promoters by varying the conveyor speed to achieve the appropriate copper removal. They are not regularly measuring the surface roughness delivered.

After soldermask application, parts for immersion silver were either processed through a jet pumice or the roughness reducing etch (RRE). The jet pumice was chosen for comparison as this is standard practice in a typical immersion silver line. For immersion tin, the parts were tested according to standard best practice. As the industry would believe roughness reduction is not necessary, performance was qualified after three levels of SMAP using only the best practice immersion tin cycles. Two market leading immersion tin processes were employed for this evaluation.

SM Prep	RRE	Jet Pumice	ImmAg	ImmSn
Standard		√	√	
				√
SMAP High		√	√	
	√		√	
				√
SMAP Med		√	√	
	√		√	
				√
SMAP Low		√	√	
	√		√	
				√

Figure 9: Test Matrix

After completion of manufacture, parts were brought to an assembly line for solder paste printing and lead free reflow. Panels were not populated with components due to cost restraints.

Thickness Measurements by XRF

Silver thickness measurements were taken using a Fischerscope XDV-SDD (silicon drift detector) Pin diode XRF unit [13]. It is well documented that immersion plating processes will plate thicker deposits on smaller pads and thinner on larger pads. This is the nature of all displacement reactions. It can be mitigated to some extent but not eliminated, by carefully controlling the processing bath operating parameters and the equipment used for plating. All silver thickness measurements were uniform from panel to panel and within the panel on varied pad sizes as shown in figure 10.

For the immerison tin panels it was more accurate to measure tin thickness by SERA as plated and after one lead free reflow excursion. It was necessary to take thickness measurements as and after reflow as will be shown later because the solderablity performance was signifcantly different. This is expected with immerison tin as discussed earlier due to the loss of pure tin to intermetallic growth after heat treatment.

Both chemcial processes resulted in very similar pure tin thickness as plated, about 0.85 microns regardless of copper roughness. Figures 11 and 12 confirm that after one lead free reflow the amount of pure tin is reduced by about 75%. The amount of pure tin lost was not effected by the starting copper roughness or the resultant tin roughness.

SM Prep	RRE	Jet Pumice	60x80 mil	Mounting hole	Delta
Standard		√	**11.2**	**9.8**	**0.13**
SMAP High		√	**10.8**	**11.1**	**0.03**
	√		**10.8**	**10.1**	**0.06**
SMAP Med		√	**9.2**	**10.1**	**0.10**
	√		**10.8**	**9.8**	**0.09**
SMAP Low		√	**10.0**	**10.6**	**0.06**
	√		**11.0**	**9.1**	**0.17**

Figure 10: Immersion silver thickness measurements

SM Prep	As	1x reflow	Delta
Standard	**0.868**		
SMAP High	**0.857**	**0.225**	**0.702**
SMAP Med	**0.876**	**0.260**	**0.703**
SMAP Low	**0.853**	**0.213**	**0.750**

Figure 11: Immersion tin (A) thickness measurements

SM Prep	As	1x reflow	Delta
Standard	**0.854**		
SMAP High	**0.862**	**0.264**	**0.694**
SMAP Med	**0.853**	**0.255**	**0.701**
SMAP Low	**0.857**	**0.250**	**0.708**

Figure 12: Immersion tin (E) thickness measurements

Surface Roughness

Panels were measured for Ra and RSAR using the Zygo profilometer. The same size surface pads is measured 5 times over three separate arrays from one 18"x24" starting panel. Figure 13 shows how the surface appearance viewed by SEM compares to the quantitative roughness figures produced by the Zygo. The measurements listed in figure 13 are on the copper surface after soldermask pretreatment. For consistency, roughness, thickness and performance was analysis on side A or the component side of the panels for all testing.

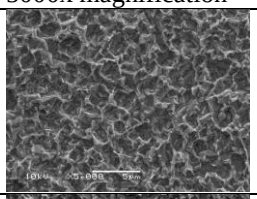
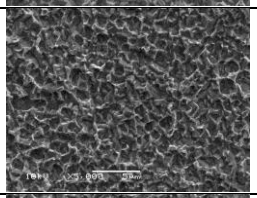
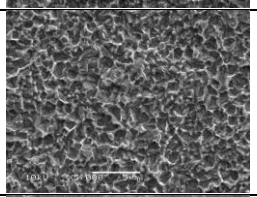
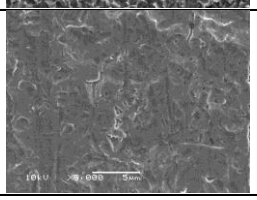
Conveyor Speed	SEM 5000x magnification	Ra	RSAR
2.0m/min		0.5564	0.4053
3.2m/min		0.4801	0.3636
4.0m/min		0.3846	0.2901
Standard Brush + etch		0.0787	0.11396

Figure 13: SEM appearance and zygo measurements after soldermask pretreatment

Figure 14 illustrates the surface roughness both visually and quantitatively after the incoming copper was processed through the roughness reducing etch.

Another comparison can be made using figure 15 which shows how the roughness compares after the SMAP, RRE and jet pumice, respectively.

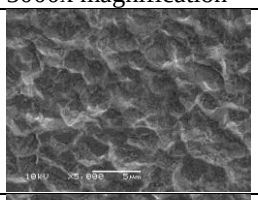
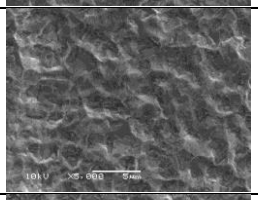
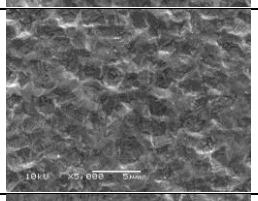
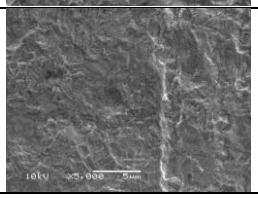
Conveyor Speed	SEM 5000x magnification	Ra	RSAR
2.0m/min		0.2235	0.1574
3.2m/min		0.2000	0.1229
4.0m/min		0.1548	0.0854
Standard Brush + etch		0.1363	0.0525

Figure 14: SEM appearance and zygo measurements post roughness reduction

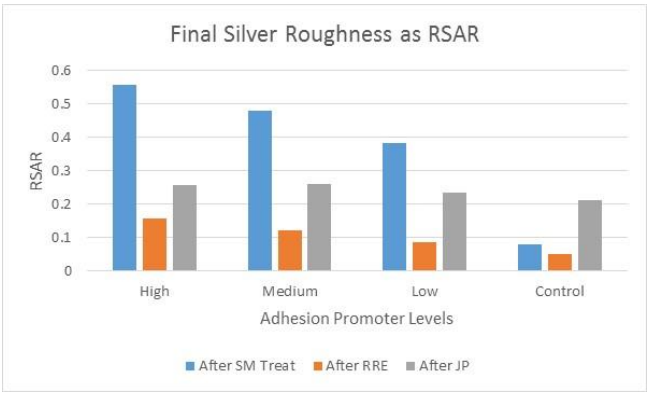


Figure 15: Zygo measurements after silver plating comparing two roughness reduction styles

The plated silver surface with either reduction step shows an RSAR less than 0.25, the RRE was more effective at reducing surface roughness than a jet pumice cycle. The quality of the solderability was not affected by the roughness of the silver once the copper was altered. As was proven in the previous publication some roughness reduction is necessary but RSAR on the order of 0.25 or lower will produce quality solder joints and solder wetting. Solder results will be discussed in more detail in the following section.

The immersion tin samples had a much more unique and unexpected set of results relating to surface roughness but still tracked with the hypothesis that end roughness on a surface finish effects solderability performance. Again, measurements were taken post tin plating as viewed in figure 16.

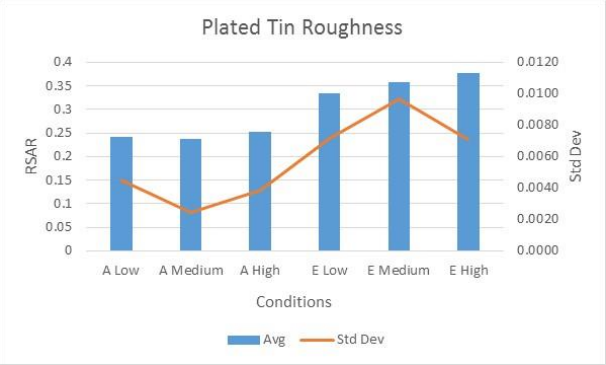


Figure 16: Zygo measurements after tin plating

For the A set of tin panels, the post tin plating roughness was all very similar regardless of the incoming copper surface condition. The E set overall had a higher roughness than A and tracked well with the incoming copper surface condition. As the copper roughness increased, the finished tin roughness increased. SEM images were taken to determine if the roughness differences could also be observed visually. Surprisingly, the tin grain structures were dramatically different but the roughness from low to high delivered by the SMAP could not be detected by this method.

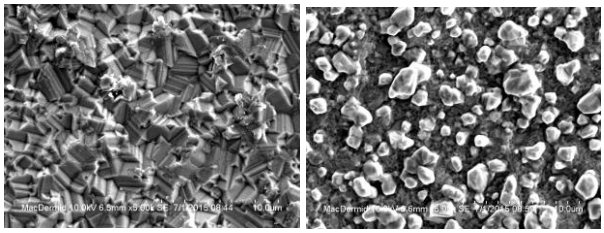


Figure 17a: SEM of A immersion tin
Figure 17b: SEM of E immersion tin

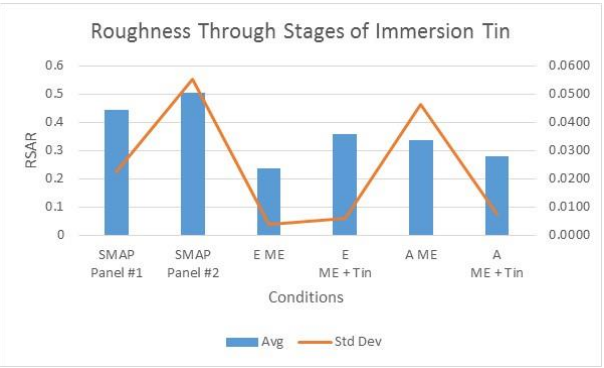


Figure 18: Zygo measurements after tin plating stages

Surface roughness was then measured after each process step in the immersion tin cycle to determine how well the microetch for each supplier was reducing the incoming copper versus how the tin grain structure itself was effecting resultant roughness. Note, the standard deviation of roughness delivered by the SMAP is very high. This should be monitored in production and again, is reason for concern, further demonstrating that creating such a significant roughness may not be consistent over a production size panel.

Again, if the parts were kept to a roughness less than 0.25 such as when a standard soldermask pretreatment is used all solderability is good and any roughness introduced by the tin grain structure is still successful.

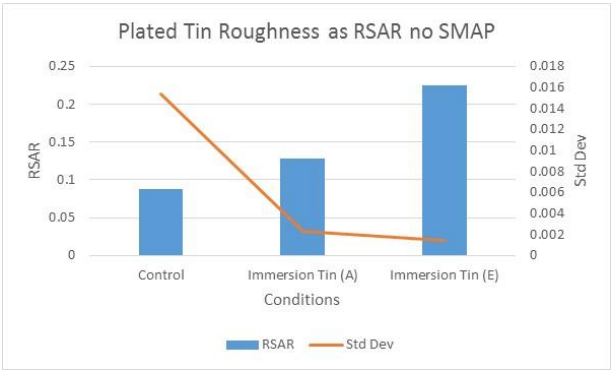


Figure 19: Zygo measurements after tin plating no SMAP

Solderability

All immersion silver circuits were shipped directly from fabrication to an assembly facility where they were automatically printed with lead free solder and processed on a convection style reflow oven using the solder paste recommended reflow profile. The production board was a single side surface mount style. All panels and features showed uniform solderability. No differences could be observed on wetting.

Assembly Method

- Solder alloy: Sn96.5 Ag3.0 Cu0.5
- Heller 1809 MKIII reflow oven
- Peak temperature: 250°C
- Flux type: Koki S3X58-M650-2 ROL0

The immersion tin samples were not processed through the same pilot scale run as the immersion silver due to the need for understanding after one lead free reflow exposure. For the immersion tin, two larger pads areas were chosen for solder spread testing. Small 60 x 80mil rectangles were printed on the boards then reflowed and solderability was assess. This was again replicated after a set of panels had been exposed to one lead free reflow prior to pasting to assess second side spread.

Solder Spread Method

- Solder alloy: Sn96.5 Ag3.0 Cu0.5
- Virtoncs XPM^2 Reflow Oven
- Peak temperature: 245°C
- Flux type: Kester EM907 ROL0

Overall, all samples as plated had very good solder spread. The small rectangles flowed past their printed area in all cases (see figure 20). The A set had so much solder flow, that the individual printed rectangles flowed together. Greater differences between the various SMAP levels was observed on the samples exposed to one reflow before printing. Of course a reduction from the "as plated" parts to those after reflow was expected. Not much spread difference could be observed on the A set. It can be stated that the highest roughness incoming copper resulted in the least spread of the three but the difference was not large. This likely is as a result of the relative uniformity in the surface roughness after tin plating. All samples had very similar RSAR numbers, (figure 16). Interestingly the E set showed much greater solder spread differences. On the low copper roughness the rectangles flowed past their printed area leaving a plump, rounded shape. The highest roughness did not display spread. The rectangles remained in their printed area and on some edges, the solder pulled back slightly. It was not a full solder reflow.

Figure 20a: Solder spread: as plated tin (E) with low SMAP
Figure 20b: Solder spread: reflowed tin (E) with low SMAP
Figure 20c: Solder spread: reflowed tin (E) with high SMAP

The solder spread data strongly correlates to the roughness measurements found on the E set. With increased roughness there was a decrease in solder spread. When roughness was maintained below 0.25 as a result of using a reduction step post soldermask adhesion promoter or when conventional cycles were used, the E set soldered well with uniform flow.

Soldermask Adhesion Testing

Two separate tests were performed to evaluate the adhesion of the soldermask to the copper surface as explored in the first publication. The failure mode for immersion tin and immersion silver are different but both share the same level of inconsistency. They depend on the quality of the soldermask process. When conventional soldermask adhesion promoters such as brush or pumice scrubbing are used, evidence of soldermask deterioration can be seen in the form of lifting at the interface either after chemical processing or heat treatments.

With immersion tin's propensity to chemically attack soldermask parts were subjected to the standard IPC tape testing to determine any soldermask lifting or embrittlement. All immersion tin panels passed without any removal of soldermask regardless of etch depth used in the adhesion promoter.

It is not usual for immersion silver chemistry to attack soldermask due to it being a strongly acidic plating system. An alternate method to determine the adhesion of soldermask for immersion silver processed parts is to analyze the area where a metal pad or trace meets the soldermask area. This is called the soldermask interface. Parts were stripped of the mask using a caustic and solvent based solution. The samples were then analyzed optically to determine any reduction in trace width or height. A design susceptible to this type of attack was used for the test. Figure 21 shows a distinct line of delineation between the areas where soldermask was covering the trace versus where it was not. In this darkened line, there is removal of copper and the trace height has been compromised. Figure 22 on the other hand shows only a color difference between where the silver has plated compared to the copper trace. There is no degradation of the copper that was right at the soldermask edge. This further proves that the soldermask was well adhered to the copper substrate and did not allow for any solution entrapment or chemical attack. There was no noticeable soldermask interface attack on any of the SMAP levels evaluated.

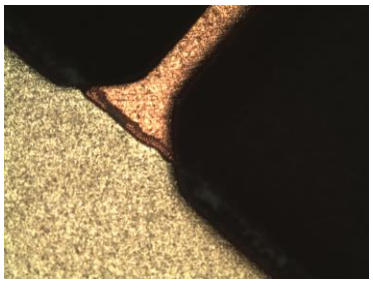


Figure 21: Soldermask interface after mask removal on immersion silver with conventional brush SM pretreatment

Figure 22: Soldermask interface after mask removal on immersion silver with proprietary SM pretreatment (SMAP)

Three dimensional optical imaging enables one to view the defect with clearer understanding of how the area is being etch and provides a quantitative measurement for the reduction of copper trace area.

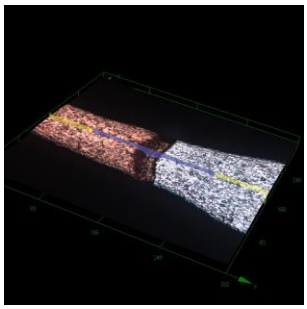


Figure 23: Soldermask interface after mask removal on immersion silver with conventional brush SM pretreatment

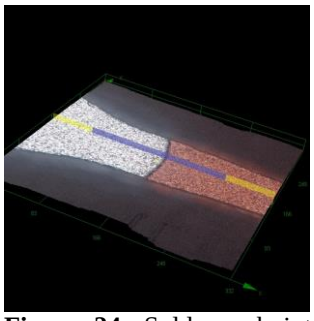


Figure 24: Soldermask interface after mask removal on immersion silver with proprietary SM pretreatment (SMAP)

The instrument is calibrated to show the trace reduction either by height or width. In this case any loss was a function of height. The control, no soldermask adhesion promoter shows a reduction of 6 microns in a design and process flow susceptible to soldermask interface attack. The same plating process conditions but with the use of the SMAP shows the reduction is essentially nothing on most samples or less than a micron in the worst instance. It is a dramatic improvement over the control.

ID	Width[µm]	Height[µm]	Length[µm]
Low	164.905	0	164.905
Medium	164.905	0.065	164.905
High	164.905	0.858	164.907
Contol	76.838	6.139	77.083

Figure 25: Trace reduction measurements at the soldermask interface area

CONCLUSIONS

In conclusion, we have described a process that allows for the use of heavy roughness soldermask adhesion promoters without detriment to the expected performance of the subsequently applied immersion metal surface finish. The benefits of soldermask adhesion promoters are detailed and the enhancement of solderability is seen with the further use of the proposed roughness reducing steps. Testing and further evaluations are ongoing with key OEMs and fabrication houses.

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