COPPER PILLAR PLATING SYSTEMS
HIGH SPEED - LOW HEAT

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ABSTRACT
This present paper deals with the ever-more stringent requirements of to-date Interconnect Technologies (ICT) from die through final assembly in particular as far as digital and analog high frequencies, undistorted signal propagation and efficient heat propagation are concerned. From waferlevel packaging to the finished Printed Circuit Board copper pillars, solid copper posts (with Printed Circuitry it´s copper filled Through Holes respectively) continue to play a vital role in coping with high speed/frequency and high wattage of sub and final assemblies.

Commonly used packaging concepts comprising waferlevel plating, through-silicon-vias (TSV), redistribution layer design (RDL), intermediate pillars, macrobumps and copper filled through holes in the final circuitry are being roughly sketched followed by an overlook of the extremely different pillar geometries within each packaging level posing individual challenges on the copper plating chemistry and process. Practical aspects namely dialling in the chemistry additives and process windows to match the relevant applications´ needs will be shortly reported, the ongoing R&D work targeted for current and future requirements to be presented.This paper concludes with actual research results on achievable copper textures and the subsequent performance of the plated copper interconnects as far as crystal lattices, and the related thermal reliability are concerned.

Key words: copper pillar plating, thermal vias, plating additives, copper texture, copper reliability

INTRODUCTION
Chasing the Speed - Coping with Heat
Stunning die architectures and thus the ubiquitous subsequent miniaturization throughout any overall electronic assembly continue to gather momentum on the basic current and future challenges on Interconnect Technology (ICT) namely

- Signal (analog & digital) frequencies up to 100 GHz, even beyond
- Heat generation up to 150 W/cm^2
- Utilization of 3-D structures (component stacks)
- Mitigation of conductor parasitics (straight metal connects vs wirebonds)
- Effective heat paths leading from single "hot" components through the assembly to the environment

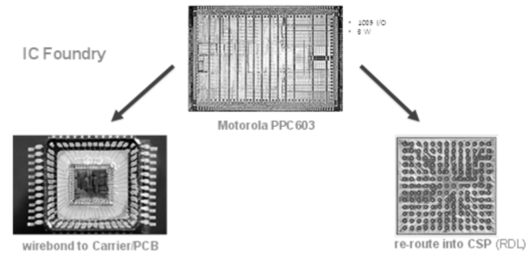

Figure 1. Wirebond and Redistribution scheme

Starting from the Integrated Circuit (IC) foundry the first packaging step would be either wirebonding a naked die to a carrier/Printed Circuit Board (PCB) **or** re-routing the die-pads (I/Os) into a chip-size- or chip-scale package (CSP) utilizing one side of a die as a Redistribution Layer (RDL). Any carrier (aka interposer) as well as CSP may be fitted with connecting metal studs, pillars, bumps thus providing the option for 2.5D or 3D stacking not to mention the final soldering of Ball-Grid-Arrays (BGA) to a Printed Circuit.

For ease of illustration and clarity any (repeated) three-dimensional "component" stacking procedures are intentionally left off in Figure 1.

The following Figure 2 shows the subsequent packaging steps onto carriers prior to component soldering to the Printed Circuit Board.

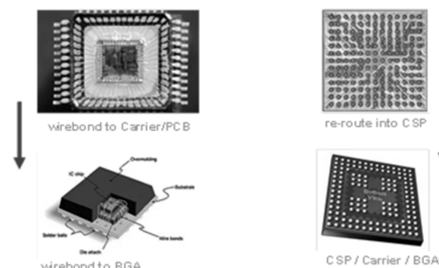

Figure 2. Stepping forward to subsequent soldering onto Printed Circuits

An example of a full 3D stackup will be presented later. The following table 1 represents – schematically - the possible measures to effectively dissipate the heat, i.e. conducting the excessive power from any die through the various packaging steps to the environment.

Table 1. Various measures of heat dissipation at various packaging levels

Packaging level	Measure for Heat Conduction	Thermal Conductivity z-axis
wirebonded dies	thermal adhesives, metal core / backed substrates	5 – 10 W/mK
CSP (~ stacked)	designed in thermal/GND pads, copper studs, pillars, bumps	Up to 390 W/mK
BGA Carrier, Interposer, Substrate (silicon, glass, organic)	thermal vias , thermal THs , copper filled metal core /backed substrates	Up to 390 W/mK 5 – 10 W/mK
PCB	thermal vias , thermal THs , copper filled metal core /backed substrates	Up to 390 W/mK 5 – 10 W/mK

Thus utilizing (already designed-in) thermal/GND pads on silicon may provide a seamless and most effective heat path from die through the final assembly on a Printed Circuit Board – if the interconnects on each packaging level are performed by copper studs, pillars, bumps – thermal vias and through-holes filled with copper on PCB level respectively.

Besides any heat dissipation effects said copper studs, pillars, bumps , copper filled thermal vias and through-holes do provide the shortest, extremely reliable, least parasitics´ afflicted electrical interconnects.

As being depicted in Figure 3, advanced die designs even utilize forced heatflow practises (PELTIER effect) to additionally cool down hot chips through copper & solder interconnects – again copper filled vias and/ or through holes become mandatory for utmost thermal effectivity.

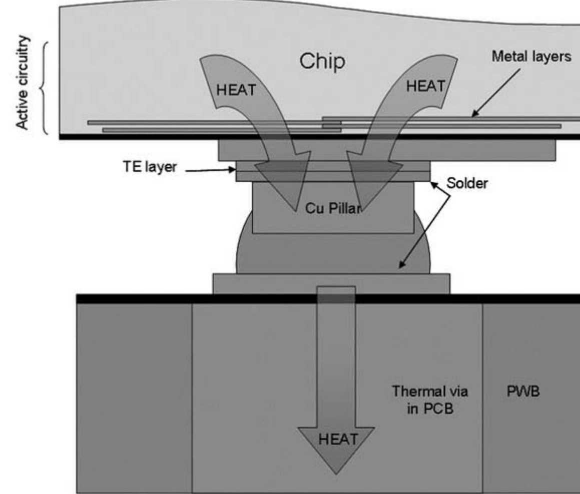

Figure 3. Forced heatflow by Peltier elements (source: nextreme)

For clarity of demonstration Figure 3 shows only one of the needed P-layer / N-layer twin pillars needed for driving the Peltier effect.

Even some mobile phone generations back Figure 4 as given very below illustrates the –seeing it historically – still breathtaking complexity of a smartphone processor package.

- Found
  - 28nm, 1.3GHz
  - 1GB LPDDR3 as PoP (64-bit)
  - Top package has 456 balls @0.35mm pitch
- ~14 x 15.5 x 1.0mm PoP
  - ~1330 balls @ 0.4mm pitch
  - LDP/TMV PoP with die back side exposed
  - Molded underfill
- 10.3 x 9.9mm die
  - 95µm thick
  - 150/170µm Sn bump pitch
  - 65µm bump height, 75µm bump diameter
- 2-2-2 substrate
  - 360µm thick
  - 75µm vias, 27µm L/S
  - Laser via in glass reinforced core
  - 25µm dielectric and copper thickness

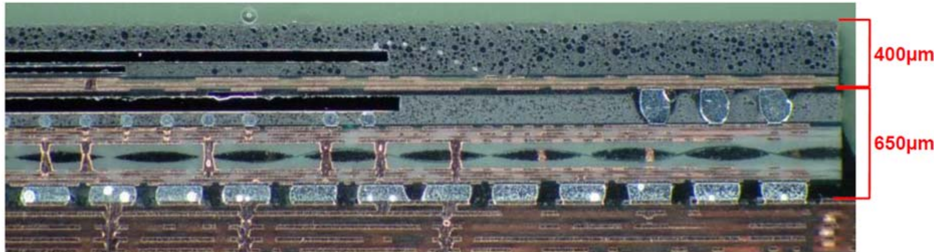

Photo source: Prismark/Binghamton University

Figure 4. From Die through Environment – full packaging complexity

From Foundry thru Assembly

Therefore providing a seamless electrical and thermal path from bare die to the final assembly´s environment already starts with the design of an Integrated Circuit and continues by designing in high performing bumps, pillars, studs, vias subsequently on interposers, carriers, substrates, Printed Wiring Boards as being sketched in the following Figure 5.

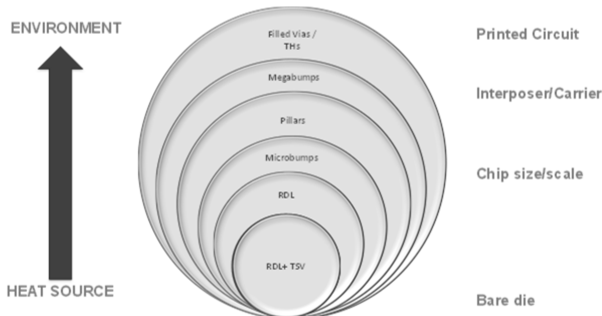

Figure 5. The seamless speedy copper path

At each design stage extremely different circuit and interconnect dimensions – application specific – do apply, ranging from µm to mm values – see Table 2 below.

These far spanned geometries – like being visualized in Figure 6 below – do require different electrolytes, different process conditions and carefully adjusted equipment ("tools") for copper plating pillars, studs, bumps, filled vias/through holes.

Table 2. Typical dimensions and applications along the Interconnect seam

Feature	Plating attributes	Diameter, L/S	Height	Package	Feature on	Application
RDL						Memory + AP / baseband
Microbump		<30 µm	<20 µm	2.5D & 3D IC	Wafer	HMC, FPGA
Cu pillar		30 - 60 µm	30 - 50 µm	FC & 2.5D	Wafer	CPU, APU, baseband, DDR4 SDRAM
Cu pillar		60 - 80 µm	50 - 70 µm	FC & 2.5D	Wafer	Power Amplifier
Large bump		90 - 110 µm	40 - 60 µm	FC & 2.5D	Wafer	FPGA
High Cu Pillar		110 - 200 µm	130 - 180 µm	PoP	Substrate	Memory + AP / baseband
Mega bump		200 µm	200 µm	3D fan out	Wafer	Memory + AP / baseband
Via / TH fill	dimple,surface thk, speed	75 - 400 µm	< 0.8 mm	assembly	Carrier / PCB	unlimited
3 in 1						

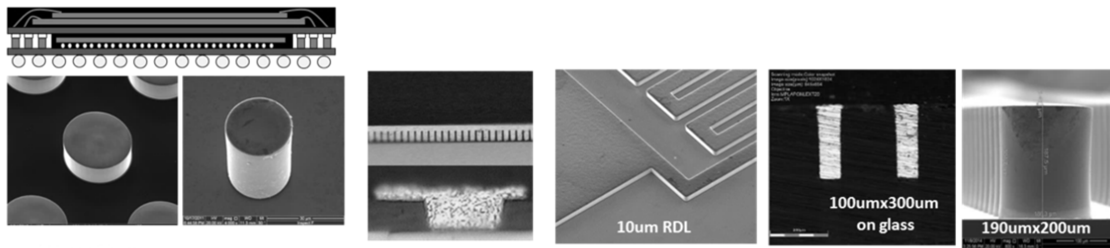

Figure 6. Different geometries requiring different chemistry/process parameters/ tools for copperplating

Geometry & Chemistry

The already cited various and extremely different geometries do simultaneously have specific requirements on **performance**, namely

- Coplanarity (Current density, feature density, etc.)
- Bump shape modulation (Chemistry selection, bump opening)

and – as always everyone´s target- on **cost reduction** as being impacted by

- Plating speed: from 2µm to 4µm/min and beyond
- Bath Life: Photoresist compatibility, additives´ by-products

The following table 3 summarizes critical attributes and the various bump shapes being – again – application specific.

Table 3. Critical attributes / bump shapes for various plating applications

Applications	Critical Plating Attribute	Bump shape
RDL	Coplanarity	Flat to domed on flat substrate
Microbumps	Coplanarity	Flat on passivation substrates, but domed on flat substrates
Cu Pillars	Coplanarity at high speed (≥3.5 µm/min)	Flat on passivation substrates, but domed on flat substrates
Macro Bumps	Bump Shape Control & speed	Flat to domed on passivation substrates
Mega Bumps	Coplanarity, very high speed (>6 µm/min)	Flat to dished, to slightly domed on flat substrates
Filled via / TH	"Post" Shape Control & speed	Flat to dished, low surface copper

It has to be stated that a one-fits-all application chemistry and its needed equipment configuration will be hard to find – if at all.

So before diving into the depth of copperpillar technologies and the related development routines a closer look at the generic hydrodynamics of any pillar feature during electroplating / filling is being sketched below in Figure 7.

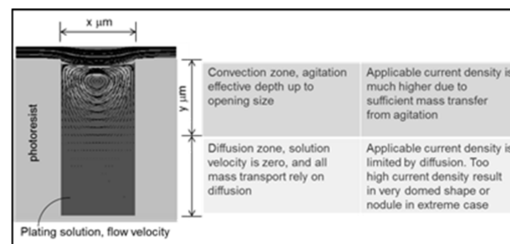

Figure 7. Diffusion zone and limiting current govern any pillar copperplating

Developing the adequate plating chemistry (additives, basic concentrations copper/sulfuric acid/chloride) with respect to plating current density and plating equipment (hydrodynamics) is basically being performed for any type of interconnect geometry (µm to mm range) by using voltammetry and/ or chronopotentiometry as the most powerful tool for any startup qualification, reference is made to Figure 8.

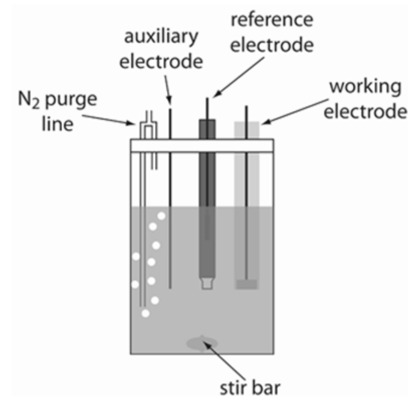

Figure 8. Schematic of a Voltammeter

Typical state-of-the-art basic copper electrolytes (aka Virginal Makeup Solution, VMS) consist of coppersulfate, sulfuric acid plus chloride ion, the latter may also be regarded as an accelerating active additive controlling the lattice and grain buildup of the electroplated copper. Concentrations in a particular VMS need to be adjusted to any geometry´s requirements, they do govern the magnitude of the limiting current and thus the final plating speed as well as the geometrical perfection of the needed copper feature.

The (**Butler-Volmer** based) equation does apply

$$i_{limiting} = \frac{nFD}{\delta} C^*$$

n = ion charge	C* = ion concentration
F = Faraday constant	δ = thk diffusion layer
D = Diffusion coefficient	

Typical additives -influencing lattice geometries - to a VMS are suppressors (wetting copper surfaces, controlling diffusion), activators (refining grain sizes by proliferation of nuclei) and, most important the so-called levellers caring for feature uniformity, feature shape, reference is made to Table 4 below.
Details of Kirkendall-void aspects will be presented later in this paper.

Table 4. Bath constituents controlling feature attributes

Attributes	Electrochemistry	Primary control	Secondary control
Bump height uniformity	High Tafel slope (W_a)	Leveller	H^+, current density, temp, Cl^-
Flat bump shape	Minimal difference in polarization between high and low agitation (Δ E)	Leveller and suppressor	Cu^{2+}, Cl^-, agitation

For any particular copper feature / geometry the best suited leveller - in concert with the other bath constituents and additives (see above) needs to be designed to its best molecular constitution and qualified by said electrochemical methods.

The achievable throwing power, i.e. degree of uniformity of the macroscopic current distribution can be predicted and application specific characterized by the Wagner number $\mathbf{W_a}$

$$W_a = \frac{\text{activation resistance}}{\text{ohmic resistance}} = \frac{R_a}{R_\Omega} = \frac{\kappa}{\ell}\left(\frac{\partial \eta_a}{\partial i}\right) = \frac{\kappa}{\ell}\frac{\beta}{i}$$

κ : electrolyte conductivity
l: distance between anode and cathode
β : Tafel slope

$\mathbf{W_a}$ and its "mathematical predecessor" the Tafel slope β do both basically represent the slope in the potential/current diagram of a given electrolyte and control in the end the domain where a leveller can be successfully applied (see Figure 9).

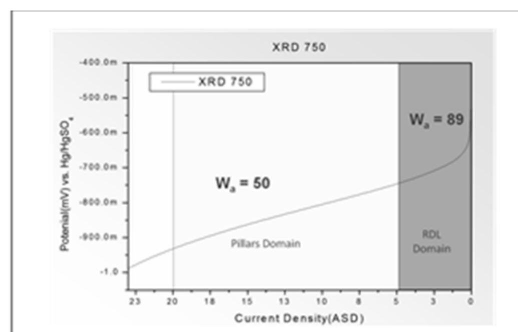

Figure 9. Characterizing designed levellers by Voltammetry

When designing and synthesizing new leveller compounds chronopotentiometry (see Figure 10) allows for rapid characterization and - much more important – for a reliable prediction of the bottom-up-fill capability (go or no-go discrimination) needless to mention that a VMS suitable for the relevant geometry / copper feature has already been composed.

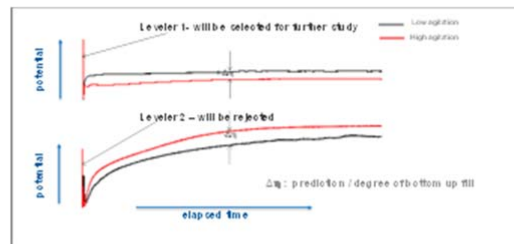

Figure 10. Leveller selection and qualification (chronopotentiometry)

Any leveller reducing the electrochemical potential at high agitation as compared to low agitation will be basically suited for bottom-up fill because of „directing" the plating current into the feature to be filled. (i.e. preferential deposition at low current density areas)

Dialling in the application

Once the VMS has been chosen for and the needed/suited additives have been designed and prequalified the subsequent task is now to determine the optimum concentrations of brightener, leveller, carrier.

Figure 11 shows an example of a leveller´s characteristic. Its growing concentration does not impact the limiting current but considerably influences the bump/ pillar uniformity - in particular Within Die (WID) and Within Feature (WIF) numbers of bump heights.

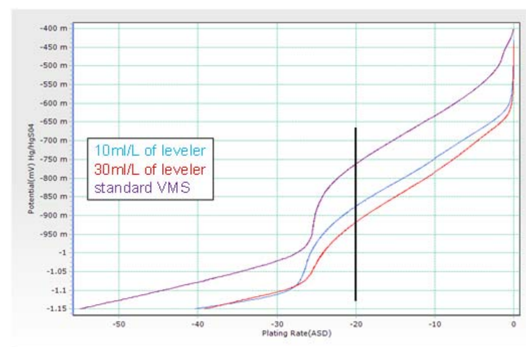

Figure 11. Leveller concentration and limiting current

Again – different bath concentrations do yield different „polarographs" and need to be dialled into the envisaged plating tool and the planned application (TSV, RDL, pillars, bumps, filled through holes) not to mention the

optimum flooding and the best substrate agitation (Figure 12).

The terms “strong“ , “weak“ , “weak to strong“, stand for any additive´s relative magnitude of its accelerating, suppressing, leveling power.

In the end of the day its not only the Voltammetry / Chronopotentiometry helping to design and qualify any particular chemistry for a given application/ geometry / tool but exhaustive designed experiments regarding

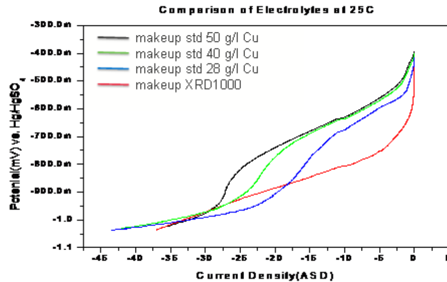

Figure 12. Application specific bath type selection

Typical electrochemical criteria for copperplating – speaking in terms of activity of the single components are listed below (Table 5).

Table 5. Dialling in the application

Process	[Cu] g/L	Accelerator	Suppressor	Leveler
Megabumps	80-90	Strong	Strong	Strong
Pillars	40-50	Strong	Weak-Strong	Strong
Microbumps	10-30	Strong	Strong	Weak
RDL	10-20	Strong	Strong	Weak-Strong
RDL + TSV	40-50	Weak	Weak-Strong	Weak-Strong

Copper Textures & Performance

Out of the manifold of possible copper lattices (see last chapter of this paper) the configuration as being named 1,1,1 – per Bravais classification/ Miller Indices – has proven to be the most preferred when speaking in terms of hardness / elongation and therefore reliability (Figure 13).

When flawlessly packed to each other these basic bi-pyramidal cells build up to socalled nano-twinned columnar structures (1) being almost insensitive to the formation of Kirkendall voids (2) in intermetalic solder layers. More literature on Kirkendall is being referenced in the appendix of this paper (3)-(6).

- Chemistry / concentrations
- Current density
- Temperature
- Tool selection
- Tool auxiliaries

including evolutionary operation need to be performed - therefore it becomes evident
that one-fits-all bath composition may still be a mere vision.

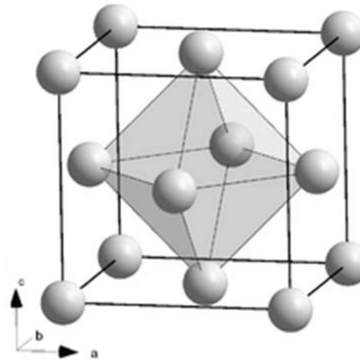

Figure 13. Always preferred – the 1,1,1 copper lattice

Void generation happens in a two-way direction: vacancies move towards the copper “substrate“ and copper ions diffuse in the opposite way – 10* faster than tin does, particularily on soldering.
The relevant thermodynamics governing the void formation are shown in Figure 14.

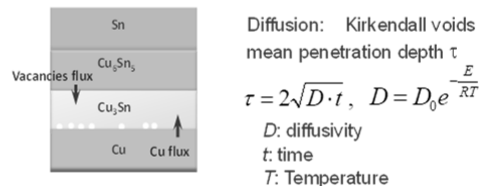

Figure 14. Thermodynamics of Kirkendall Formation

It´s the same factors cited above, namely

- Chemistry/conc. (additives per se)
- Current density
- Temperature
- Tool selection
- Tool auxiliaries

which do foster a perfect and flawless 1,1,1 copper cell unit being resistant to Kirkendall void generation.

The worst case scene in Figure 15 has been deliberately chosen for.

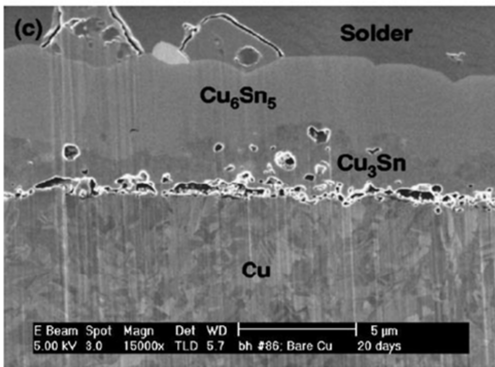

Figure 15. Kirkendall voids in intermetallic solder layers

Naturally any given impurities (e.g. carbon based , by-products, any contaminants) may lead to lattice distortions/ defects as well thus preventing a flawless 1,1,1 copper cell formation.

The Macro PCB Section – Via Fill & TH plating (7),(8)

Travelling the road from die to the final PCB
Figure 16 shows a perfectly filled Blind Microvia (BMV , size 5*3 mils) and a simultaneously copper plated Through Hole (TH dia 8 mils).

Figure 16. PCB via fill and TH plating

The development and engineering work uses the same routines as for macropillars, as already described above.
For reasons of final qualification the solid "copper post" in the BMV was routinely subjected to SEM / XRD to check for the distribution of the prevalent Bravais lattices -some basic unit cells are depicted in Figure 17.

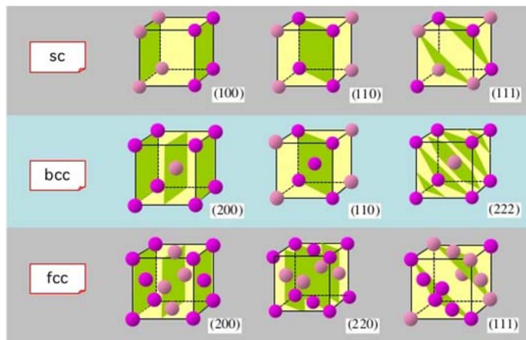

Figure 17. Basic metal lattices

Again – the preferrable and utmost reliable target is the 1,1,1 configuration (see Figure 13, above).Typically on annealing copper at elevated temperatures (e.g. 150 °C, 2 hr) the proportions of the monitored lattices may substantially change, the degree of the latter does also impact the overall copper performance.
Shown in Table 6 are the achievable crystal data of a Viafill (VF) and Through-Hole (TH) electrolytic copper plating bath.

Table 6. Copper Cristallography of a VF-TH copper plating bath (relative intensities in %)

Various data	Lit. Value Cu	Fill Cu	Fill Cu annealed
111	100	100	100
200	46	39.5	35.4
220	20	17.6	15.2
311	17	6.4	7.9
Lattice constant a [Å]	3.615	3.613	3.612
Density [g/cm³]	8.92	8.948	8.959
Stress [Mpa]	----	-5.5 ± 3.2	1.9 ± 3.1

Perfect 1,1,1 unit cells being grown to flawless copper grains and subsequent voidfree cristallites are shown in Figure 18 - it's a Scanning Electron Micrograph of an ion-milled (FIB) copperlayer being subsequently subjected to XRay Defraction (XRD) for the above mentioned copper cristall data aquisition.This configuration does not tend to undergo the vacancy-copperflux Kirkendall mechanism.

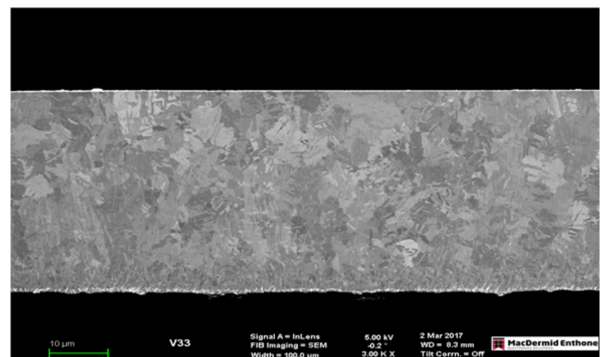

Figure 18. Perfect and void free VF-TH Copper cristallization

The Macro PCB Section – TH Bridge & Fill

A novel bridge and fill process has been developped consisting of a first electroplating step to bridge through holes in substrates / PCBs followed by a second step of filling the generated "virtual" blind vias (the latter process like the one being presented beforehand). Figure 19 shows the demarcation line between the two coppers (its a 0.25 / 0.20 mm hole in a 0.25 mm thick substrate).

Figure 19. Two-step bridge & fill of TH´s

The overall process not only fills through holes with extremely thermal conductive copper (λ = 390 W/mK)

thus providing the seamless copperpath from die through the environment but also offers the chance to cost effectively replace some staggered blind via layups by (simply) through drilled multilayers.

Designing in a strong levelling performance of the bridging electrolyte the cristalline majority of preferrable 1,1,1 unit cell has been traded off against a required minimum copper thickness at the substrate´s surface (see Table 7).

Table 7. Copper Cristallography of a bridging copper plating bath

Various data	Lit. Value Cu	Bridge Cu	Bridge Cu annealed
111	100	56.1	26.3
200	46	75.5	45.8
220	20	100	100
311	17	28.8	16.7
Lattice constant a [Å]	3.615	3.612	3.612
Density [g/cm³]	8.92	8.956	8.960
Stress [Mpa]	----	61.9 ± 3.1	-40.5 ± 3.2

The achieved inherent reliability of the composite bridge&fill copper has been demonstrated by exhaustive elongation and tensile strength testing (see Table 8).

Accordingly the related SEM micrograph shows lesser discernible grain boundaries, even some "pico"-voids, those do not impact the total hole´s IMC reliability because of the bridge copper being covered by the 2nd step fill copper thus not being in contact with an IMC layer on soldering. (ref Figure 20).

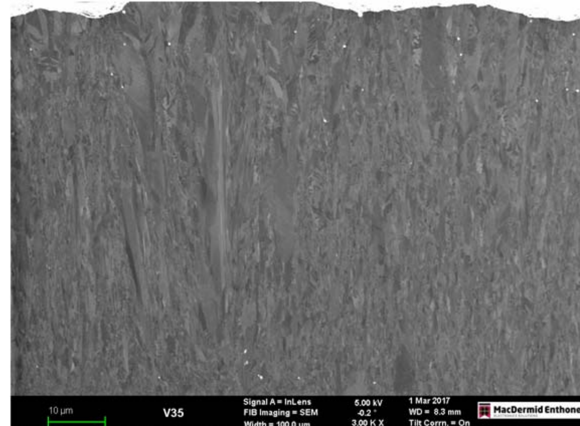

Figure 20. SEM picture of bridge copper only (FIB ion milled specimen)

Table 8. Elongation and Tensile testing of bridge&fill copper system

RUN	sample #	break force (N)	weight (g)	elongation (%)	tens. strength (kN/cm^2)	appr thk (µm)
Test 1	1	310,6	0,973	21,92	32,45	71,6
	2	360,5	1,115	21,19	32,86	82,0
	3	298,0	0,935	20,79	32,40	68,8
	4	311,3	0,990	19,46	31,95	72,9
	5	337,2	1,051	22,47	32,60	77,5
	Mean	**323,5**	**1,013**	**21,17**	**32,45 (46 kPSI)**	**74,7**
Test 2	1	304,7	0,958	19,69	32,31	70,6
	2	308,5	0,966	22,4	32,44	71,1
	3	344,8	1,075	20,82	32,60	79,2
	4	318,5	0,996	19,88	32,49	73,4
	5	312,2	0,977	22,82	32,49	71,9
	Mean	**317,7**	**0,994**	**21,12**	**32,47 (46 kPSI)**	**73,2**

Bridged & filled through holes even pass all related IPC class 3 thermal tests, including solderability, thermal shock, thermal cycling, solder dip / solder float, IST, HAST etc..

Representative for the reliability tests being performed is Figure 21 showing a flawless and perfect microsection after 6* solder shocking (288 oC, 10 s each) of a bridged&filled hole (dia 150 µm).
Current two-step capabilities (hole size versus substrate thickness) are presented in Table 9 and Table 10 showing needed plating times and achievable surface copper thicknesses

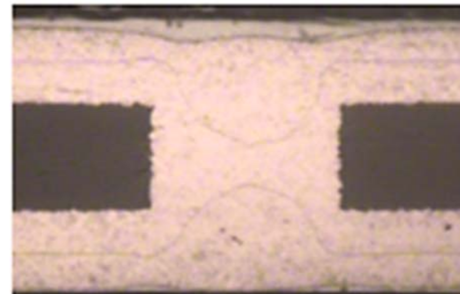

Figure 21. Solder shocking two coppers

Table 9. Through hole filling capability (bridge&fill)

Systek THF Capability Chart												
Hole diameter	0.10mm	√	√	√	√	√	√	√				
	0.15mm			√	√	√	√	√	√			
	0.20mm			√	√	√	√	√	√			
	0.25mm			√	√	√	√	√	√	√	√	
	0.30mm			√	√	√	√	√	√	√	√	√
	0.35mm			√	√	√	√	√	√	√	√	√
	0.40mm				√	√	√	√	√	√	√	√
	0.45mm									√	√	
	0.50mm										√	
		0.10mm	0.15mm	0.20mm	0.25mm	0.30mm	0.35mm	0.40mm	0.45mm	0.50mm	0.80mm	1.0mm
		Panel Thickness										

Table 10. Through hole filling capability (bridge&fill) , plated surface Copper thk and total plating time

Systek THF Capability Chart												
Hole diameter	0.10mm	3um-30min	3um-30min	5um-1hr	5um-1hr	5um-1hr	10um-2hr	10um-2hr				
	0.15mm			5um-1hr	5um-1hr	10um-2hr	10um-2hr	10um-2hr	10um-2hr			
	0.20mm			5um-1hr	5um-1hr	15um-2hr	15um-2hr	15um-2hr	20um-2hr			
	0.25mm			8um-1hr	8um-1hr	20um-2hr	20um-2hr	20um-2hr	20um-2hr	15um-1hr	15um-1hr	
	0.30mm			10um-1hr	10um-1hr	20um-2hr	20um-2hr	20um-2hr	20um-2hr	20um-2hr	20um-2hr	30um-4hr
	0.35mm			10um-1hr	10um-1hr	20um-2hr	20um-2hr	20um-2hr	20um-2hr	22um-3hr	22um-3hr	30um-4hr
	0.40mm				15um-2hr	15um-2hr	20um-2hr	20um-2hr	20um-2hr	25um-3hr	25um-3hr	35um-4hr
	0.45mm									25um-3hr	25um-3hr	
	0.50mm										25um-3hr	
		0.10mm	0.15mm	0.20mm	0.25mm	0.30mm	0.35mm	0.40mm	0.45mm	0.50mm	0.80mm	1.0mm
		Panel Thickness										

The Macro PCB Section
– Extreme Pillars at Work CONCLUSION

By concluding this paper an impression of the overall challenges of pillar plating is given by Figure 22.
Seeing it from a bird´s eye of view it takes all disciplines namely

- Additives design
- E-chemistry
- Hydrodynamics
- Equipment / CD regime

to achieve the desired copper plating performance providing seamless electrical and thermal pathes

…….from Die to Environment…..

Figure 22. Impression of Pillar Plating works

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